METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE CHANNELS AND STRUCTURE THEREOF

Abstract of the Disclosure

A transistor (10) overlies a substrate (12) and has a plurality of overlying channels (72, 74, 76) that are formed in a stacked arrangement. A continuous gate (60) material surrounds each of the channels. Each of the channels is coupled to source and drain electrodes (S/D) to provide increased channel surface area in a same area that a single channel structure is conventionally implemented. A vertical channel dimension between two regions of the gate (60) are controlled by a growth process as opposed to lithographical or spacer formation techniques. The gate is adjacent all sides of the multiple overlying channels. Each channel is formed by growth from a common seed layer and the source and drain electrodes and the channels are formed of a substantially homogenous crystal lattice.